Listing of Claims

1. (Currently Amended) A queue assignment apparatus for a communications system, comprising:

a queue which stores data for multiple links;

a queue assignment unit that assigns storage banks in the queue to the links;

a signal detection unit that detects availability of a line interface unit; and

a data control unit that reads data from the queue and writes the data in the line interface unit according to the availability of the line interface unit, wherein the queue assignment unit assigns a plurality of storage banks to at least one of the links and reallocates assignments of the storage banks to the links based on a change in load of one or more of the links, and wherein none of the storage banks is assigned to a link if the link is determined not to be in use, so as to ensure that the storage banks in the queue are assigned to links that are in use

~~wherein the queue includes at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links, and wherein an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address~~.

2. (Canceled)

3. (Canceled)

4. (Original) The apparatus of claim 1, wherein said queue assignment unit compares the number of links and the number of banks and assigns at least one bank to each link.

5. (Currently Amended) The apparatus of claim 1, wherein said signal detection unit generates ~~at least one of~~ an empty signal ~~and~~ or a full signal for a bank in the queue corresponding to each link, and reports the state of the bank to the queue assignment unit and the data control unit, the data control unit reading data from ~~and~~ or writing data to the bank based on generation of the empty signal or full signal.

6. (Currently Amended) A queue assignment apparatus in a mobile communication system, comprising:

a circuit to write data for a plurality of links in a queue of an access pointer controller, the queue including a plurality of banks for storing data for the links;

a circuit to report state information indicating whether data has been written into or read from each of the banks in the queue; ~~and~~

a circuit to write the data read from one of the banks into a FIFO memory within a line interface unit so that the data may be transmitted to an access pointer, and

an assignment circuit to assign the plurality of banks to the links, the assignment circuit to assign at least two banks to at least one of the links and to reallocate assignments of the banks to the links based on a change in load of one or more of the links, and wherein the assignment circuit assigns none of the banks to a link if the link is determined not to be in use, so as to ensure that the banks in the queue are assigned to links that are in use ~~wherein the queue~~

~~is formed from at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links~~.

7. (Currently Amended) A queue assignment method in a mobile communication system, comprising:

assigning a plurality of banks in a queue to store data for multiple links;

if data is to be written in a specific link, writing the data in the relevant bank based on a write address and a write enable signal;

increasing the address of the queue and transmitting write pointer corresponding to the address to a signal detection unit;

comparing a read pointer and the write pointer and then generating an empty signal or a full signal for transmission to a data control unit; and

depending on availability of a line interface unit and an empty state of the queue, reading data from the queue and writing it in the line interface unit, wherein said assigning includes assigning at least two banks to at least one of the links, said method further comprising reallocating assignments of the banks to the links based on a change in load of one or more of the links, wherein none of the banks are assigned to a link if the link is determined not to be in use, so as to ensure that the banks in the queue are assigned to links that are in use ~~wherein the queue includes at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links~~.

8. (Currently Amended) The method of claim 7, wherein said assigning of banks comprises:

selecting a first link, checking whether the link is in use, and if the link is in use, checking whether a second link is in use and increasing a link count until a last link is checked;

~~if the first link is not in use, assigning a desired number of banks to the first link and assigning a start address and an end address to the link;~~ and

assigning one or more banks to the second link by increasing a start address and end address of the second link by referring to the end address of the first preceding link.

9. (Previously Presented) The method of claim 7, wherein the writing comprises:

initializing address-related parameters of each link from a first link to a last link;

if the initialization is completed through the last link, starting a read algorithm;

checking whether there exists one item of data to be written in the queue beginning with the first link until the last link has been checked;

if there exists data to be written, writing the data using a write address and write enable signal and increasing a total address when the writing is completed;

setting a write pointer with the increased total address, transmitting the write pointer to a signal detection unit and checking whether a current address of the link is the highest address of the bank by referring to the total address; and

if the current address is the highest address, toggling write carry for the next link, assigning the lowest bits to the total address, or if the current address is not the highest address, checking whether there is data for the next link.

10. (Original) The method of claim 9, wherein said address-related parameters include a link start address, a link end address, a total address, and a write carry.

11. (Original) The method of claim 9, wherein when the current address of the link has not reached the highest address of the bank, if the restart condition arises, said flexible queue assignment method further comprises initializing address-related parameters of each link.

12. (Original) The method of claim 7, wherein generating the empty signal comprises:

determining a range of each link;

from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference between write pointer and read pointer; and

checking existence of data based on the difference of the pointers and generating the empty signal accordingly.

13. (Original) The method of claim 12, wherein said range of each link indicates a number of banks assigned to each link and is determined by using a start address and an end address of each link.

14. (Original) The method of claim 7 wherein generating the full signal comprises:

determining a range of each link;

from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference of pointers according to the comparison; and

if the write carry and the read carry are the same, generating the full signal indicating a full or not-full state depending on whether said difference of pointers is within certain user-specified range.

15. (Original) The method of claim 14, wherein said difference of pointers is calculated by subtracting the read pointer from the write pointer if the write pointer and the read pointer are the same, or if the write pointer and the read pointer are not the same by calculating the difference of the write pointer and the read pointer reflecting the range of link.

16. (Original) The method of claim 7, wherein said reading of data from the queue comprises:

checking whether the empty signal is in the not-empty state from the first link to the last link;

if a link is detected to be in the not-empty state, reading data through read address and read enable signal connected to the queue;

increasing read address and total address by the number of data items that have been read and checking whether the current address of the link is equal to the highest address of the bank; and

if the current address of the link is equal to the highest address, toggling read carry and initializing total address with the lowest address of the bank, thereby moving to a next link.

17-20 (Canceled)

21. (New) The apparatus of claim 1, wherein:

the queue includes at least one dual-port random access memory (DPRAM);

the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links, and

an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address.

22. (New) The apparatus of claim 6, wherein the queue is formed from at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links.

23. (New) The method of claim 7, wherein the queue includes at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links.